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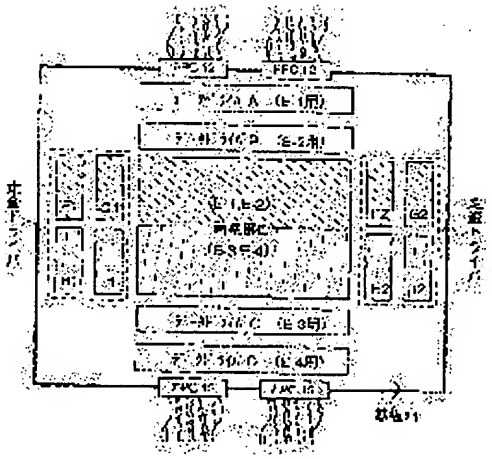
(54) DISPLAY DEVICE AND DRIVING METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To solve the problem that a write time is made insufficient due to enlargement and resolution enhancement of a display device.

SOLUTION: In the display device and a driving method therefor, x data lines (x is a natural number equal to or larger than 4) are arranged for each column, and video signals can be simultaneously supplied to x pixels through x data lines respectively. Video signals can be simultaneously supplied to x pixels in contrast to the conventional dot sequential driving in which signals are supplied individually to pixels, and video signals can be simultaneously supplied to (x×n) in contrast to the conventional line sequential driving in which signals are supplied to n pixels from the first column to the last column (the n-th column in this case). Thus the write time of video signals to pixels can be x times as long as that in conventional methods.



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CLAIMS

[Claim(s)]
[Claim 1]
It has the picture element part by which two or more pixels have been arranged,
The display characterized by arranging the four or more data lines for every train at said picture element part.
[Claim 2]
It has the picture element part by which two or more pixels have been arranged,
The display characterized by arranging the two or more data lines at each of two or more of said pixels.
[Claim 3]
In claim 2,
Said pixel is equipped with the component for switching, and a light emitting device,
Said component for switching is a display characterized by connecting with any one data line defined for every pixel between said two or more data lines, and not connecting with other data lines.
[Claim 4]
Two or more pixels to which each has two or more scanning lines in two or more data lines and a line writing direction, and has a light emitting device in the direction of a train at a list are the displays arranged in the shape of a matrix,
The x data lines (x is the four or more natural numbers) are arranged for every train among said data lines which are books, and the one scanning line is arranged for every line among said two or more scanning lines,
Said y scan drivers which choose two or more x scanning lines as coincidence among the scanning lines of a book (y is the one or more natural numbers),
The display characterized by having x data drivers which supply a signal at coincidence in x pixels chosen from said two or more pixels through each of said x data lines arranged for every train.
[Claim 5]
Two or more pixels in which it is arranged in the one scanning line and the list which have been arranged for every x data line (x is the four or more natural numbers) arranged for every train and train at the intersection of said data line and said scanning line, and each has a light emitting device are the displays by which two or more arrangement was carried out at the shape of a matrix,
Said y scan drivers which choose two or more x scanning lines as coincidence among the scanning lines of a book (y is the one or more natural numbers),
The display characterized by having x data drivers which supply a signal at coincidence in x pixels chosen from said two or more pixels through each of said x data lines arranged for every train.
[Claim 6]
In claim 4 or 5,
Each of said x data drivers is a display characterized by having a sampling circuit corresponding to each of two or more shift registers which operate independently, respectively, and two or more of said shift registers.

[Claim 7]
In claim 4 or 5,
Each of said x data drivers is a display characterized by having a sampling circuit in the 1st latch and the 2nd latch list corresponding to each of two or more shift registers which operate independently, respectively, and two or more of said shift registers.
[Claim 8]
In claim 3 thru/or any 1 term of 5,
Said light emitting device is a display characterized by being OLED.
[Claim 9]
In claim 4 or 5,
It is the display characterized by said y scan drivers and said x data drivers being formed by said two or more pixel lists on the same insulator.
[Claim 10]
In claim 4 or 5,
The display characterized by having the capacity object which holds said video signal in the transistor for a switch which controls the input of the video signal over the transistor for a drive which controls the current value of said light emitting device, and said pixel in said pixel, and a list.
[Claim 11]
In claim 4 or 5,
The display characterized by having the transistor for elimination which discharges the charge held at the capacity object which holds said video signal in the transistor for a switch which controls the input of the video signal over the transistor for a drive which controls the current value of said light emitting device, and said pixel in said pixel, and a list, and said capacity object.
[Claim 12]
Two or more pixels to which each has a light emitting device in two or more data lines of the direction of a train and two or more scanning lines of a line writing direction, and a list are arranged in the shape of a matrix,
The x data lines (x is the two or more natural numbers) are arranged for every train among said data lines which are books, and it is said drive approach of a display that two or more one scanning line has been arranged for every line among the scanning lines of a book,
An one-frame period has two or more subframe periods,
Each of two or more of said subframe periods has an elimination period in a write-in period and a luminescence period or a write-in period, and a luminescence period list,
It is the drive approach of the display characterized by supplying a signal to coincidence at x pixels chosen from said two or more pixels through each of said x data lines which the x scanning lines were chosen as coincidence by y scan drivers (y is the one or more natural numbers), and have been arranged by x data drivers for every train in said write-in period.
[Claim 13]
The pixel which is arranged in the one scanning line and the list which have been arranged for every x data line arranged for every train and train at the intersection of said data line and said scanning line, and has a light emitting device is the drive approach of the display by which two or more arrangement was carried out at the shape of a matrix,
An one-frame period has two or more subframe periods,
Each of two or more of said subframe periods has an elimination period in a write-in period and a luminescence period or a write-in period, and a luminescence period list,
It is the drive approach of the display characterized by supplying a signal to coincidence at x pixels chosen from said two or more pixels through each of said x data lines which the x scanning lines were chosen as coincidence by y scan drivers (y is the one or more natural numbers), and have been arranged by x data drivers for every train in said write-in period.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
This invention relates to the display which used the light emitting device, especially, is large-sized and belongs to the technical field of the display of high resolution.
[0002]
[Description of the Prior Art]
In recent years, the importance of the display which performs the display of an image has been increasing increasingly. The liquid crystal display which displays an image, using a liquid crystal device as a current display is broadly used taking advantage of high definition, the thin shape, and which lightweight advantage. Moreover, development of the display (luminescence equipment) using light emitting devices, such as organic light emitting diode (OLED:Organic Light Emitting Diode), as other displays is also furthered. The luminescence equipment (OLED display) using OLED excels [speed of response / besides the above-mentioned advantage which the existing liquid crystal display has] in a movie display quickly, has the descriptions, like a visual field property is large, and attracts attention greatly. OLED which is the typical light emitting device adopted as luminescence equipment is having structure of having the thin film of a monolayer thru/or a laminating, between a conductive anode plate and cathode, and an organic material is contained in the part or all the layers of this thin film. It is usually that the brightness and current value of organic light emitting diode fill the relation of direct proportion.
[0003]
Luminescence equipment shall have below two or more pixels which have a light emitting device (for example, OLED) and at least two transistors in the shape of a matrix. In a pixel, it is the transistor connected with the light emitting device at the serial, and what controls the brightness of a light emitting device writes it as the transistor for a drive. Although the video signal of an electrical potential difference or a current format is used for control of a pixel, in using the signal of an electrical-potential-difference format, a signal level is usually inputted into the gate electrode of the transistor for a drive, and it controls the brightness of a light emitting device using this transistor for a drive. In using the signal of a current format, it controls the brightness of this light emitting device by supplying the current equivalent to the predetermined signal current to a light emitting device from the transistor for a drive. In addition, the case (an analog drive is called below) where a video signal uses the signal of an analog value in spite of which of an electrical-potential-difference format and a current format, and the signal of digital value may be used (a digital drive is called below). In a digital drive, it is combinable with the area gradation drive (for example, refer to application for patent No. 382530 [2001 to]) which expresses middle gradation in the form of the time-sharing drive (for example, JP,2001-5426,A) expressed in the form of a time amount ratio, or surface ratio. Since it is high-speed as compared with liquid crystal etc., the speed of response of OLED is suitable for the time-sharing drive of a digital drive.

[0004]
The picture element part of the display which performs the here conventional matrix display, and the outline of a drive circuit are shown in drawing 7 . A picture element part consists of two or more data lines arranged in the direction of a train which intersects perpendicularly with two or more scanning lines and lines which have been arranged at the line writing direction to which a horizontal scanning is performed, and two or more pixels arranged in the shape of a matrix at the list. Thus, two or more pixels are arranged regularly at a picture element part, and the one data line is arranged for every one scanning line and train for every line [further].
[0005]
[Problem(s) to be Solved by the Invention]
If frame frequency is fixed, 1 horizontal-scanning period will become short with high-resolution-izing of a picture element part. For example, if the number of pixels becomes [frame frequency] SXGA specification (1280x1024) by 60Hz, 1 horizontal-scanning period will serve as 16microsec. extent. In such a case, it is not easy to secure the write-in time amount of the video signal over a pixel. This inclination is remarkable when it is the display of the large-sized screen where the parasitic capacitance especially to wiring becomes large.
[0006]
The case of being concrete is examined. First, a video signal does not ask a current value format or an electrical-potential-difference value format, but considers the case of digital time-sharing gradation. For example, when dividing one frame into 15 subframe extent and performing a time-sharing drive, 1 horizontal-scanning period in case the number of pixels is SXGA specification (1280x1024) becomes below 1microsec. typically, and write-in time amount runs short.
Next, the case of the analog drive using the video signal of a current value format is considered. When the video-signal current supplied to a light emitting device displays small low brightness gradation, drawing speed becomes remarkably slow, it writes in actually, and time amount runs short.
[0007]
This invention is made in view of an above-mentioned technical problem, and let it be a technical problem to offer the display which canceled the lack of write-in time amount produced with enlargement and high-resolution-izing of a display, and its drive approach. Especially this invention makes it a technical problem to offer the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the video signal of a current value format by a digital time-sharing drive or analog drive.
[0008]
[Means for Solving the Problem]
in order to solve the above-mentioned technical problem -- this invention -- the x data lines (x is the four or more natural numbers) per train -- arranging -- this -- the display which can supply a video signal to x pixels through each of the x data lines at coincidence, and its drive approach are offered. This invention makes it possible to supply a video signal for the place which supplied the signal for every pixel by the point sequential drive conventionally to x pixels at coincidence. Furthermore, the display which made it possible to supply a video signal for the place which supplied the signal to n pixels of up to the last train (here, the last train is set with n train) from [one train] at coincidence at the pixel of an individual (xxn), and its drive approach are conventionally offered by line sequential drive. This becomes possible in this invention to make write-in time amount of the video signal over a pixel into a x times as many ratio as this conventionally.
[0009]
This invention is a display with which two or more pixels which each has two or more scanning lines in two or more data lines and a line writing direction, and have a light emitting device (typically organic light emitting diode, OLED) in the direction of a train at a list have been arranged in the shape of a matrix,
It is characterized by said thing [that two or more x data lines (x is the four or more natural numbers) are arranged for every train among the data lines of a book].

[0010]
A data driver is arranged to the upper and lower sides of each, and this invention can be applied, also when operating independently the pixel in the upper half of a screen, and the pixel in the lower half of a screen and writing in a video signal (a vertical division drive is called hereafter). In this case, if it doubles under a top, the number of the data line per train can be used as a book (2xx) (x is the two or more natural numbers).
[0011]
This invention which has the above-mentioned configuration offers the display which canceled the lack of write-in time amount produced with enlargement and highly-minute-izing of a display, and its drive approach. Especially this invention offers the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the signal of a current value format by a digital time-sharing drive or analog drive.
[0012]
[Embodiment of the Invention]
(Gestalt 1 of operation)
This invention is explained using drawing 1 -3, and 8, 9, 13 and 14.
[0013]
Drawing 1 is first used and explained about the example of a configuration of the display of this invention. A display has the picture element part E formed on the substrate 11, and has the data driver (here four data driver A-D) and scan driver (eight scan drivers F1-I1, F2-I2) which have been arranged further around this picture element part E. The pixel E-1 in the upper half of a screen drives the pixel E-2 A, F1, F2, and in the upper half of a screen by B, G1, and G2. The pixel E-3 in the lower half of a screen drives the pixel E-4 C, H1, H2, and in the lower half of a screen by D, I1, and I2 similarly.
In addition, although premised on the vertical division drive with this gestalt, this vertical division drive is not indispensable to operation of this invention. However, the reservation of the write-in time amount of a video signal to a pixel is more effectively performed by combining with this invention.
[0014]
A signal is supplied to data driver A-D and the scan drivers F1-I1, and F2-I2 from the exterior through FPC12. In addition, the above-mentioned driver may be formed on a substrate 11, and may be arranged outside as another IC. Moreover, especially the number of the above-mentioned driver is not limited, but can be set up according to the configuration of a pixel etc. However, as for the number of a data driver, it is desirable that it is the same as the number of the data line arranged for every train. Moreover, although the picture element part E was divided roughly into four fields E-1 to E-4 here, this invention is not limited to this but may be divided roughly into how many fields.
[0015]
In addition, with an indicating equipment, the module which mounted IC etc. in the panel which enclosed the picture element part and drive circuit which have a light emitting device between a substrate and covering material, and said panel, the display used as a monitor of a personal computer are included in criteria. That is, with an indicating equipment, it is equivalent to generic names, such as a panel, a module, and a display.
[0016]
Although four gestalten are explained about the example of a configuration of a picture element part E here, the 1st configuration is first explained using drawing 13 (A). In drawing 13 (A), two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the two data lines and each pixel in the line writing direction. With this gestalt, a picture element part is divided in the center, the data lines SA and SB are arranged in a screen upper half, and the data lines SC and SD are arranged in a screen lower half. And it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB]. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.

[0017]
And on the left-hand side of a screen, the scan drivers F1-I1 are arranged, and the scan drivers F2-I2 are arranged on the right-hand side of a screen. And selection of a pixel E-1 is performed by the scan drivers F1 and F2 from the direction of both the left-hand side of a screen, and right-hand side. The same is said of the other pixels E-2 to E-4.
In addition, although it is not necessary to necessarily arrange a scan driver on both sides of a screen, it can raise the selection rate of a pixel by arranging on both sides of a screen compared with the case of one side. Therefore, as for a scan driver, in the indicating equipment of the high resolution of a big screen with which especially a load becomes heavy, arranging on both sides of a screen is desirable.
The lack of write-in time amount produced since the parasitic capacitance remarkable in the display of a large-sized screen to wiring of this invention which has the above-mentioned configuration is large is cancelable.
[0018]
Here, in the upper half of [screen] a picture element part E, it assumes that the pixel of an individual is arranged in the pixel of an individual, and a screen lower half (nxm) (ixj), and the configuration of four pixels E-1 to E-4 arranged at a coordinate (i, j-1), (i, j), (n, m-1), and (n, m) is explained using drawing 13 (B) and (C). In addition, since it can design freely, the circuitry of a pixel shows only the component for switching, and a light emitting device all over drawing and in a pixel.
Each of four pixels shown in drawing 13 (B) and (C) is controlled by different data-line SA-SD. Therefore, the four scanning lines G (j-1)-Gj which control a pixel E-1 to E-4, and G (m-1)-Gm become possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing. It becomes possible to supply a signal to x pixels at coincidence about the place which supplied the signal for every pixel when it was degree drive. that that is right, then the former -- a dot order -- If it is furthermore a line sequential drive conventionally, it will become possible to supply a signal to the pixel of an individual (xxn) at coincidence about the place which supplied the signal to coincidence at n pixels of up to the last train (here, the last train is set with n train) from [one train]. By this configuration, it becomes possible to raise the write-in time amount over a pixel, and the lack of write-in time amount can be canceled.
In addition, drawing 13 (C) shows the case where the scanning line is carried out in common between the adjoining pixels. This invention may share the scanning line between the pixels which adjoin for improvement in a numerical aperture in order to arrange two or more signal lines in one train.
[0019]
Subsequently, the 2nd configuration is explained using drawing 2 . In drawing 2 , two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the four data lines and each pixel in the line writing direction. And it writes SA-SD [the four data lines arranged at one train], and it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the above-mentioned gestalt] here.
[0020]
Subsequently, it illustrates using drawing 2 (B) and (C) about the example of a configuration of four pixels E-1 to E-4 arranged at coordinate (i. j) - (i, j+3). Each of four pixels shown in drawing 2 (B) and (C) is controlled by different data-line SA-SD. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.
[0021]
Subsequently, the 3rd configuration is explained using drawing 8 . In drawing 8 (A), two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the two data lines and each pixel in the line writing direction. With this gestalt, a picture element part is divided in the center and SC and SD are arranged in the data lines SA and SB and a screen lower half at a screen upper half.

And it writes SD [the data line controlled by SC and the data driver D in the data line controlled by SB and the data driver C in the data line controlled by SA and the data driver B in the data line controlled by the data driver A]. Moreover, it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the 1st and 2nd gestalt of the above]. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.

[0022]

Here, the configuration of a pixel E-1 to E-4 is shown in drawing 8 (B) and (C). Each of four pixels shown in drawing 8 (B) and (C) is controlled by different data-line SA-SD. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.

[0023]

Subsequently, the 4th configuration is explained using drawing 14 . In drawing 14 , two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the four data lines and each pixel in the line writing direction. And it writes SA-SD [the four data lines arranged at one train], and it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the above-mentioned gestalt] here. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.

[0024]

Here, each of four pixels of E-1 to E-4 shown in drawing 14 (B) and (C) is controlled by different data-line SA-SD about the configuration of E-4 from a pixel E-1. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.

[0025]

Subsequently, the example of the above-mentioned scan method of the 1st - the 4th configuration is explained using drawing 9 . The 1st configuration shown in drawing 9 (A) and drawing 13 about the 3rd configuration shown in drawing 8 is explained using drawing 9 (C) about the 2nd and 4th configurations shown in drawing 9 (B) and drawing 2 , and 14.

[0026]

With the 1st configuration shown in drawing 13 , a picture element part is divided roughly into two fields from [a line (m / 2+1)] to a last line eye (here, they may be m lines) even with the m/2nd line from the 1st line. The pixel by which the pixel arranged at the oddth line in the pixel arranged from the 1st line at eye a line (m / 2+1) has been arranged at the scan driver F and the eventh line is controlled by the scan driver G. (m / 2+1) The pixel by which the pixel arranged at the oddth line in the pixel arranged from eye a line at the last line eye has been arranged at the scan driver H and the eventh line is controlled by the scan driver I. And a pixel is scanned in the direction of the m/2nd line from the 1st line by the scan driver F, and a pixel is scanned from the m/4th line in the direction of the m/2nd line by the scan driver G to the same timing.

[0027]

It divides roughly into the pixel arranged among two or more pixels at eye a line [eye a line / the m-th line and / (m+1) and] (m+2) and eye a line (m+3) with the 2nd and 4th configurations shown in drawing 2 and 14. And the pixel by which the pixel by which the pixel by which the pixel arranged at the m-th line has been arranged at the scan driver F and eye a line (m+1) has been arranged at the scan driver G and eye a line (m+2) has been arranged at the scan driver H and eye a line (m+3) is controlled by the scan driver I.

[0028]

With the 3rd configuration shown in drawing 8 , a picture element part is divided roughly into four

fields from the 1st line to a last line eye (here, they may be m lines). The pixel by which the pixel arranged from the 1st line at the m/4th line has been arranged by the m/2nd line from the scan driver F and eye a line (m / 4+1) The scan driver G (m / 2+1) The pixel by which the pixel arranged by (3xm) / the 4th line from eye a line has been arranged from the {[(3xm)] 1st [/4+}] line by the scan driver H and the last line eye is controlled by the scan driver I. That is, the pixel arranged from the 1st line at the m/4th line is scanned by the scan driver F, and the pixel arranged from eye a line (m / 4+1) to the same timing at the m/2nd line is scanned by the scan driver G. (Threexm) / the 4th line is scanned by the scan driver H from the m/2nd line, and the pixel arranged by the last line eye from the {[(3xm)] 1st [/4+}] line is scanned by the scan driver I.

[0029]

Subsequently, the example of a configuration of a data driver is explained. Here, the data driver A is mentioned as an example and it explains using drawing 3 . A data driver is divided roughly into two or more fields, and operates each in parallel. Here, suppose that it is divided roughly into eight of A-1 to A-8. When the number of pixels is a color SXGA temporarily, the data line of a book is connected to each (160x (RGB)) of A-1 to A-8.

And when a data driver performs a point sequential drive, each of the data driver A-1 to A-8 has shift registers SR1-SR40 and sampling circuits SMP1-SMP40. moreover -- the case where a data driver performs a line sequential drive -- each of the data driver A-1 to A-8 -- shift registers SR1-SR40 and the 1st -- latch L1-1-L1-40 and a list -- the 2nd -- it has latch L2-1-L2-40. When the number of pixels is SXGA temporarily, the data line of a book is connected to each (4x (RGB)) of SMP1-SMP40.

[0030]

Here, actuation of the data driver of drawing 3 (B) is explained briefly. This data driver is an object for a point sequential drive, and when a video signal is the analog drive of an electrical-potential-difference format, it is suitable. The **** configuration of a flip-flop circuit (FF), the decoder, etc. is carried out for two or more trains, and each of shift registers SR1-SR40 outputs a sampling pulse one by one according to the timing of a clock (S-CLK) or a start pulse (S-SP), and supplies this sampling pulse to sampling circuits SMP1-SMP40. The video signal is inputted into sampling circuits SMP1-SMP40, and the video signal inputted into these sampling circuits SMP1-SMP40 is outputted to the data lines SA1-SA160 according to the timing of the sampling pulse inputted.

[0031]

Subsequently, actuation of the data driver of drawing 3 (C) is explained briefly. This data driver is an object for a line sequential drive, and, in the digital time-sharing drive, is suitable. A shift register outputs a sampling pulse one by one, as mentioned above, and this sampling pulse is supplied to sampling circuits SMP1-SMP40 (1st latch L1- 1- L1 -40). The video signal is inputted into sampling circuits SMP1-SMP40, and the video signal is held in each train to them according to the timing into which a sampling pulse is inputted.

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EFFECT OF THE INVENTION

[Effect of the Invention]
this invention -- the x data lines (x is the four or more natural numbers) per train -- arranging -- this -- the display which can supply a signal to x pixels through each of the x data lines at coincidence, and its drive approach are offered. Furthermore, this invention is arranging two or more data drivers which choose the data line. It makes it possible to supply a signal for the place which supplied the signal for every pixel by the point sequential drive conventionally to x pixels at coincidence. Furthermore, the display which made it possible to supply a signal for the place which supplied the signal to n pixels of up to the last train (here, the last train is set with n train) from [one train] at coincidence at the pixel of an individual (xxn), and its drive approach are conventionally offered by line sequential drive.
[0097]
This invention which has the above-mentioned configuration offers the display which canceled the lack of write-in time amount produced with enlargement and highly-minute-izing of a display, and its drive approach. Especially this invention offers the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the signal of a current value format by a digital time-sharing drive or analog drive.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]
If frame frequency is fixed, 1 horizontal-scanning period will become short with high-resolution-izing of a picture element part. For example, if the number of pixels becomes [frame frequency] SXGA specification (1280x1024) by 60Hz, 1 horizontal-scanning period will serve as 16microsec. extent. In such a case, it is not easy to secure the write-in time amount of the video signal over a pixel. This inclination is remarkable when it is the display of the large-sized screen where the parasitic capacitance especially to wiring becomes large.
[0006]
The case of being concrete is examined. First, a video signal does not ask a current value format or an electrical-potential-difference value format, but considers the case of digital time-sharing gradation. For example, when dividing one frame into 15 subframe extent and performing a time-sharing drive, 1 horizontal-scanning period in case the number of pixels is SXGA specification (1280x1024) becomes below 1microsec. typically, and write-in time amount runs short.
Next, the case of the analog drive using the video signal of a current value format is considered. When the video-signal current supplied to a light emitting device displays small low brightness gradation, drawing speed becomes remarkably slow, it writes in actually, and time amount runs short.
[0007]
This invention is made in view of an above-mentioned technical problem, and let it be a technical problem to offer the display which canceled the lack of write-in time amount produced with enlargement and high-resolution-izing of a display, and its drive approach. Especially this invention makes it a technical problem to offer the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the video signal of a current value format by a digital time-sharing drive or analog drive.
[0008]

[Translation done.]

* NOTICES *

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MEANS

[Means for Solving the Problem]
in order to solve the above-mentioned technical problem -- this invention -- the x data lines (x is the four or more natural numbers) per train -- arranging -- this -- the display which can supply a video signal to x pixels through each of the x data lines at coincidence, and its drive approach are offered. This invention makes it possible to supply a video signal for the place which supplied the signal for every pixel by the point sequential drive conventionally to x pixels at coincidence. Furthermore, the display which made it possible to supply a video signal for the place which supplied the signal to n pixels of up to the last train (here, the last train is set with n train) from [one train] at coincidence at the pixel of an individual (xxn), and its drive approach are conventionally offered by line sequential drive. This becomes possible in this invention to make write-in time amount of the video signal over a pixel into a x times as many ratio as this conventionally.
[0009]
This invention is a display with which two or more pixels which each has two or more scanning lines in two or more data lines and a line writing direction, and have a light emitting device (typically organic light emitting diode, OLED) in the direction of a train at a list have been arranged in the shape of a matrix,
It is characterized by said thing [that two or more x data lines (x is the four or more natural numbers) are arranged for every train among the data lines of a book].
[0010]
A data driver is arranged to the upper and lower sides of each, and this invention can be applied, also when operating independently the pixel in the upper half of a screen, and the pixel in the lower half of a screen and writing in a video signal (a vertical division drive is called hereafter). In this case, if it doubles under a top, the number of the data line per train can be used as a book (2xx) (x is the two or more natural numbers).
[0011]
This invention which has the above-mentioned configuration offers the display which canceled the lack of write-in time amount produced with enlargement and highly-minute-izing of a display, and its drive approach. Especially this invention offers the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the signal of a current value format by a digital time-sharing drive or analog drive.
[0012]
[Embodiment of the Invention]
(Gestalt 1 of operation)
This invention is explained using drawing 1 -3, and 8, 9, 13 and 14.
[0013]
Drawing 1 is first used and explained about the example of a configuration of the display of this invention. A display has the picture element part E formed on the substrate 11, and has the data driver (here four data driver A-D) and scan driver (eight scan drivers F1-I1, F2-I2) which have been arranged

further around this picture element part E. The pixel E-1 in the upper half of a screen drives the pixel E-2 A, F1, F2, and in the upper half of a screen by B, G1, and G2. The pixel E-3 in the lower half of a screen drives the pixel E-4 C, H1, H2, and in the lower half of a screen by D, I1, and I2 similarly.
In addition, although premised on the vertical division drive with this gestalt, this vertical division drive is not indispensable to operation of this invention. However, the reservation of the write-in time amount of a video signal to a pixel is more effectively performed by combining with this invention.
[0014]
A signal is supplied to data driver A-D and the scan drivers F1-I1, and F2-I2 from the exterior through FPC12. In addition, the above-mentioned driver may be formed on a substrate 11, and may be arranged outside as another IC. Moreover, especially the number of the above-mentioned driver is not limited, but can be set up according to the configuration of a pixel etc. However, as for the number of a data driver, it is desirable that it is the same as the number of the data line arranged for every train. Moreover, although the picture element part E was divided roughly into four fields E-1 to E-4 here, this invention is not limited to this but may be divided roughly into how many fields.
[0015]
In addition, with an indicating equipment, the module which mounted IC etc. in the panel which enclosed the picture element part and drive circuit which have a light emitting device between a substrate and covering material, and said panel, the display used as a monitor of a personal computer are included in criteria. That is, with an indicating equipment, it is equivalent to generic names, such as a panel, a module, and a display.
[0016]
Although four gestalten are explained about the example of a configuration of a picture element part E here, the 1st configuration is first explained using drawing 13 (A). In drawing 13 (A), two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the two data lines and each pixel in the line writing direction. With this gestalt, a picture element part is divided in the center, the data lines SA and SB are arranged in a screen upper half, and the data lines SC and SD are arranged in a screen lower half. And it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB]. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.
[0017]
And on the left-hand side of a screen, the scan drivers F1-I1 are arranged, and the scan drivers F2-I2 are arranged on the right-hand side of a screen. And selection of a pixel E-1 is performed by the scan drivers F1 and F2 from the direction of both the left-hand side of a screen, and right-hand side. The same is said of the other pixels E-2 to E-4.
In addition, although it is not necessary to necessarily arrange a scan driver on both sides of a screen, it can raise the selection rate of a pixel by arranging on both sides of a screen compared with the case of one side. Therefore, as for a scan driver, in the indicating equipment of the high resolution of a big screen with which especially a load becomes heavy, arranging on both sides of a screen is desirable.
The lack of write-in time amount produced since the parasitic capacitance remarkable in the display of a large-sized screen to wiring of this invention which has the above-mentioned configuration is large is cancelable.
[0018]
Here, in the upper half of [screen] a picture element part E, it assumes that the pixel of an individual is arranged in the pixel of an individual, and a screen lower half (nxm) (ixj), and the configuration of four pixels E-1 to E-4 arranged at a coordinate (i, j-1), (i, j), (n, m-1), and (n, m) is explained using drawing 13 (B) and (C). In addition, since it can design freely, the circuitry of a pixel shows only the component for switching, and a light emitting device all over drawing and in a pixel.
Each of four pixels shown in drawing 13 (B) and (C) is controlled by different data-line SA-SD. Therefore, the four scanning lines G (j-1)-Gj which control a pixel E-1 to E-4, and G (m-1)-Gm become

possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing. It becomes possible to supply a signal to x pixels at coincidence about the place which supplied the signal for every pixel when it was degree drive. that that is right, then the former -- a dot order -- If it is furthermore a line sequential drive conventionally, it will become possible to supply a signal to the pixel of an individual (xxn) at coincidence about the place which supplied the signal to coincidence at n pixels of up to the last train (here, the last train is set with n train) from [one train]. By this configuration, it becomes possible to raise the write-in time amount over a pixel, and the lack of write-in time amount can be canceled.
In addition, drawing 13 (C) shows the case where the scanning line is carried out in common between the adjoining pixels. This invention may share the scanning line between the pixels which adjoin for improvement in a numerical aperture in order to arrange two or more signal lines in one train.
[0019]
Subsequently, the 2nd configuration is explained using drawing 2 . In drawing 2 , two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the four data lines and each pixel in the line writing direction. And it writes SA-SD [the four data lines arranged at one train], and it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the above-mentioned gestalt] here.
[0020]
Subsequently, it illustrates using drawing 2 (B) and (C) about the example of a configuration of four pixels E-1 to E-4 arranged at coordinate (i. j) - (i, j+3). Each of four pixels shown in drawing 2 (B) and (C) is controlled by different data-line SA-SD. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.
[0021]
Subsequently, the 3rd configuration is explained using drawing 8 . In drawing 8 (A), two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the two data lines and each pixel in the line writing direction. With this gestalt, a picture element part is divided in the center and SC and SD are arranged in the data lines SA and SB and a screen lower half at a screen upper half.
And it writes SD [the data line controlled by SC and the data driver D in the data line controlled by SB and the data driver C in the data line controlled by SA and the data driver B in the data line controlled by the data driver A]. Moreover, it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the 1st and 2nd gestalt of the above]. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.
[0022]
Here, the configuration of a pixel E-1 to E-4 is shown in drawing 8 (B) and (C). Each of four pixels shown in drawing 8 (B) and (C) is controlled by different data-line SA-SD. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.
[0023]
Subsequently, the 4th configuration is explained using drawing 14 . In drawing 14 , two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the four data lines and each pixel in the line writing direction. And it writes SA-SD [the four data lines arranged at one train], and it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the above-mentioned gestalt] here. That is, the data driver B and a pixel E-3 are controlled by the data

driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.

[0024]

Here, each of four pixels of E-1 to E-4 shown in drawing 14 (B) and (C) is controlled by different data-line SA-SD about the configuration of E-4 from a pixel E-1. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.

[0025]

Subsequently, the example of the above-mentioned scan method of the 1st - the 4th configuration is explained using drawing 9 . The 1st configuration shown in drawing 9 (A) and drawing 13 about the 3rd configuration shown in drawing 8 is explained using drawing 9 (C) about the 2nd and 4th configurations shown in drawing 9 (B) and drawing 2 , and 14.

[0026]

With the 1st configuration shown in drawing 13 , a picture element part is divided roughly into two fields from [a line (m / 2+1)] to a last line eye (here, they may be m lines) even with the m/2nd line from the 1st line. The pixel by which the pixel arranged at the oddth line in the pixel arranged from the 1st line at eye a line (m / 2+1) has been arranged at the scan driver F and the eventh line is controlled by the scan driver G. (m / 2+1) The pixel by which the pixel arranged at the oddth line in the pixel arranged from eye a line at the last line eye has been arranged at the scan driver H and the eventh line is controlled by the scan driver I.

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MEANS

[Means for Solving the Problem]
in order to solve the above-mentioned technical problem -- this invention -- the x data lines (x is the four or more natural numbers) per train -- arranging -- this -- the display which can supply a video signal to x pixels through each of the x data lines at coincidence, and its drive approach are offered. This invention makes it possible to supply a video signal for the place which supplied the signal for every pixel by the point sequential drive conventionally to x pixels at coincidence. Furthermore, the display which made it possible to supply a video signal for the place which supplied the signal to n pixels of up to the last train (here, the last train is set with n train) from [one train] at coincidence at the pixel of an individual (xxn), and its drive approach are conventionally offered by line sequential drive. This becomes possible in this invention to make write-in time amount of the video signal over a pixel into a x times as many ratio as this conventionally.
[0009]
This invention is a display with which two or more pixels which each has two or more scanning lines in two or more data lines and a line writing direction, and have a light emitting device (typically organic light emitting diode, OLED) in the direction of a train at a list have been arranged in the shape of a matrix,
It is characterized by said thing [that two or more x data lines (x is the four or more natural numbers) are arranged for every train among the data lines of a book].
[0010]
A data driver is arranged to the upper and lower sides of each, and this invention can be applied, also when operating independently the pixel in the upper half of a screen, and the pixel in the lower half of a screen and writing in a video signal (a vertical division drive is called hereafter). In this case, if it doubles under a top, the number of the data line per train can be used as a book (2xx) (x is the two or more natural numbers).
[0011]
This invention which has the above-mentioned configuration offers the display which canceled the lack of write-in time amount produced with enlargement and highly-minute-izing of a display, and its drive approach. Especially this invention offers the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the signal of a current value format by a digital time-sharing drive or analog drive.
[0012]
[Embodiment of the Invention]
(Gestalt 1 of operation)
This invention is explained using drawing 1 -3, and 8, 9, 13 and 14.
[0013]
Drawing 1 is first used and explained about the example of a configuration of the display of this invention. A display has the picture element part E formed on the substrate 11, and has the data driver (here four data driver A-D) and scan driver (eight scan drivers F1-I1, F2-I2) which have been arranged

further around this picture element part E. The pixel E-1 in the upper half of a screen drives the pixel E-2 A, F1, F2, and in the upper half of a screen by B, G1, and G2. The pixel E-3 in the lower half of a screen drives the pixel E-4 C, H1, H2, and in the lower half of a screen by D, I1, and I2 similarly.
In addition, although premised on the vertical division drive with this gestalt, this vertical division drive is not indispensable to operation of this invention. However, the reservation of the write-in time amount of a video signal to a pixel is more effectively performed by combining with this invention.
[0014]
A signal is supplied to data driver A-D and the scan drivers F1-I1, and F2-I2 from the exterior through FPC12. In addition, the above-mentioned driver may be formed on a substrate 11, and may be arranged outside as another IC. Moreover, especially the number of the above-mentioned driver is not limited, but can be set up according to the configuration of a pixel etc. However, as for the number of a data driver, it is desirable that it is the same as the number of the data line arranged for every train. Moreover, although the picture element part E was divided roughly into four fields E-1 to E-4 here, this invention is not limited to this but may be divided roughly into how many fields.
[0015]
In addition, with an indicating equipment, the module which mounted IC etc. in the panel which enclosed the picture element part and drive circuit which have a light emitting device between a substrate and covering material, and said panel, the display used as a monitor of a personal computer are included in criteria. That is, with an indicating equipment, it is equivalent to generic names, such as a panel, a module, and a display.
[0016]
Although four gestalten are explained about the example of a configuration of a picture element part E here, the 1st configuration is first explained using drawing 13 (A). In drawing 13 (A), two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the two data lines and each pixel in the line writing direction. With this gestalt, a picture element part is divided in the center, the data lines SA and SB are arranged in a screen upper half, and the data lines SC and SD are arranged in a screen lower half. And it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB]. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.
[0017]
And on the left-hand side of a screen, the scan drivers F1-I1 are arranged, and the scan drivers F2-I2 are arranged on the right-hand side of a screen. And selection of a pixel E-1 is performed by the scan drivers F1 and F2 from the direction of both the left-hand side of a screen, and right-hand side. The same is said of the other pixels E-2 to E-4.
In addition, although it is not necessary to necessarily arrange a scan driver on both sides of a screen, it can raise the selection rate of a pixel by arranging on both sides of a screen compared with the case of one side. Therefore, as for a scan driver, in the indicating equipment of the high resolution of a big screen with which especially a load becomes heavy, arranging on both sides of a screen is desirable.
The lack of write-in time amount produced since the parasitic capacitance remarkable in the display of a large-sized screen to wiring of this invention which has the above-mentioned configuration is large is cancelable.
[0018]
Here, in the upper half of [screen] a picture element part E, it assumes that the pixel of an individual is arranged in the pixel of an individual, and a screen lower half (nxm) (ixj), and the configuration of four pixels E-1 to E-4 arranged at a coordinate (i, j-1), (i, j), (n, m-1), and (n, m) is explained using drawing 13 (B) and (C). In addition, since it can design freely, the circuitry of a pixel shows only the component for switching, and a light emitting device all over drawing and in a pixel.
Each of four pixels shown in drawing 13 (B) and (C) is controlled by different data-line SA-SD. Therefore, the four scanning lines G (j-1)-Gj which control a pixel E-1 to E-4, and G (m-1)-Gm become

possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing. It becomes possible to supply a signal to x pixels at coincidence about the place which supplied the signal for every pixel when it was degree drive. that that is right, then the former -- a dot order -- If it is furthermore a line sequential drive conventionally, it will become possible to supply a signal to the pixel of an individual (xxn) at coincidence about the place which supplied the signal to coincidence at n pixels of up to the last train (here, the last train is set with n train) from [one train]. By this configuration, it becomes possible to raise the write-in time amount over a pixel, and the lack of write-in time amount can be canceled.
In addition, drawing 13 (C) shows the case where the scanning line is carried out in common between the adjoining pixels. This invention may share the scanning line between the pixels which adjoin for improvement in a numerical aperture in order to arrange two or more signal lines in one train.
[0019]
Subsequently, the 2nd configuration is explained using drawing 2 . In drawing 2 , two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the four data lines and each pixel in the line writing direction. And it writes SA-SD [the four data lines arranged at one train], and it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the above-mentioned gestalt] here.
[0020]
Subsequently, it illustrates using drawing 2 (B) and (C) about the example of a configuration of four pixels E-1 to E-4 arranged at coordinate (i. j) - (i, j+3). Each of four pixels shown in drawing 2 (B) and (C) is controlled by different data-line SA-SD. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.
[0021]
Subsequently, the 3rd configuration is explained using drawing 8 . In drawing 8 (A), two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the two data lines and each pixel in the line writing direction. With this gestalt, a picture element part is divided in the center and SC and SD are arranged in the data lines SA and SB and a screen lower half at a screen upper half.
And it writes SD [the data line controlled by SC and the data driver D in the data line controlled by SB and the data driver C in the data line controlled by SA and the data driver B in the data line controlled by the data driver A]. Moreover, it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the 1st and 2nd gestalt of the above]. That is, the data driver B and a pixel E-3 are controlled by the data driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.
[0022]
Here, the configuration of a pixel E-1 to E-4 is shown in drawing 8 (B) and (C). Each of four pixels shown in drawing 8 (B) and (C) is controlled by different data-line SA-SD. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.
[0023]
Subsequently, the 4th configuration is explained using drawing 14 . In drawing 14 , two or more pixels are arranged in the shape of a matrix at a picture element part E, and further, the one scanning line passes along each pixel in the direction of a train, and they pass along the four data lines and each pixel in the line writing direction. And it writes SA-SD [the four data lines arranged at one train], and it writes E-4 [the pixel which connected to E-3 and data-line SD the pixel which connected to E-2 and data-line SC the pixel which connected the pixel linked to data-line SA to E-1 and data-line SB like the above-mentioned gestalt] here. That is, the data driver B and a pixel E-3 are controlled by the data

driver C, and a pixel E-4 is controlled [a pixel E-1] for the data driver A and a pixel E-2 by the data driver D, respectively.
[0024]
Here, each of four pixels of E-1 to E-4 shown in drawing 14 (B) and (C) is controlled by different data-line SA-SD about the configuration of E-4 from a pixel E-1. Therefore, a pixel E-1 to E-4 becomes possible [choosing it as coincidence], and, as a result, it becomes possible to write a signal in four pixels to the same timing.
[0025]
Subsequently, the example of the above-mentioned scan method of the 1st - the 4th configuration is explained using drawing 9 . The 1st configuration shown in drawing 9 (A) and drawing 13 about the 3rd configuration shown in drawing 8 is explained using drawing 9 (C) about the 2nd and 4th configurations shown in drawing 9 (B) and drawing 2 , and 14.
[0026]
With the 1st configuration shown in drawing 13 , a picture element part is divided roughly into two fields from [a line (m / 2+1)] to a last line eye (here, they may be m lines) even with the m/2nd line from the 1st line. The pixel by which the pixel arranged at the oddth line in the pixel arranged from the 1st line at eye a line (m / 2+1) has been arranged at the scan driver F and the eventh line is controlled by the scan driver G. (m / 2+1) The pixel by which the pixel arranged at the oddth line in the pixel arranged from eye a line at the last line eye has been arranged at the scan driver H and the eventh line is controlled by the scan driver I. And a pixel is scanned in the direction of the m/2nd line from the 1st line by the scan driver F, and a pixel is scanned from the m/4th line in the direction of the m/2nd line by the scan driver G to the same timing.
[0027]
It divides roughly into the pixel arranged among two or more pixels at eye a line [eye a line / the m-th line and / (m+1) and] (m+2) and eye a line (m+3) with the 2nd and 4th configurations shown in drawing 2 and 14. And the pixel by which the pixel by which the pixel by which the pixel arranged at the m-th line has been arranged at the scan driver F and eye a line (m+1) has been arranged at the scan driver G and eye a line (m+2) has been arranged at the scan driver H and eye a line (m+3) is controlled by the scan driver I.
[0028]
With the 3rd configuration shown in drawing 8 , a picture element part is divided roughly into four fields from the 1st line to a last line eye (here, they may be m lines). The pixel by which the pixel arranged from the 1st line at the m/4th line has been arranged by the m/2nd line from the scan driver F and eye a line (m / 4+1) The scan driver G (m / 2+1) The pixel by which the pixel arranged by (3xm) / the 4th line from eye a line has been arranged from the {[(3xm)] 1st [/4+}] line by the scan driver H and the last line eye is controlled by the scan driver I. That is, the pixel arranged from the 1st line at the m/4th line is scanned by the scan driver F, and the pixel arranged from eye a line (m / 4+1) to the same timing at the m/2nd line is scanned by the scan driver G. (Threexm) / the 4th line is scanned by the scan driver H from the m/2nd line, and the pixel arranged by the last line eye from the {[(3xm)] 1st [/4+}] line is scanned by the scan driver I.
[0029]
Subsequently, the example of a configuration of a data driver is explained. Here, the data driver A is mentioned as an example and it explains using drawing 3 . A data driver is divided roughly into two or more fields, and operates each in parallel. Here, suppose that it is divided roughly into eight of A-1 to A-8. When the number of pixels is a color SXGA temporarily, the data line of a book is connected to each (160x (RGB)) of A-1 to A-8.
And when a data driver performs a point sequential drive, each of the data driver A-1 to A-8 has shift registers SR1-SR40 and sampling circuits SMP1-SMP40. moreover -- the case where a data driver performs a line sequential drive -- each of the data driver A-1 to A-8 -- shift registers SR1-SR40 and the 1st -- latch L1-1-L1-40 and a list -- the 2nd -- it has latch L2-1-L2-40. When the number of pixels is SXGA temporarily, the data line of a book is connected to each (4x (RGB)) of SMP1-SMP40.

[0030]
Here, actuation of the data driver of drawing 3 (B) is explained briefly. This data driver is an object for a point sequential drive, and when a video signal is the analog drive of an electrical-potential-difference format, it is suitable. The **** configuration of a flip-flop circuit (FF), the decoder, etc. is carried out for two or more trains, and each of shift registers SR1-SR40 outputs a sampling pulse one by one according to the timing of a clock (S-CLK) or a start pulse (S-SP), and supplies this sampling pulse to sampling circuits SMP1-SMP40. The video signal is inputted into sampling circuits SMP1-SMP40, and the video signal inputted into these sampling circuits SMP1-SMP40 is outputted to the data lines SA1-SA160 according to the timing of the sampling pulse inputted.
[0031]
Subsequently, actuation of the data driver of drawing 3 (C) is explained briefly. This data driver is an object for a line sequential drive, and, in the digital time-sharing drive, is suitable. A shift register outputs a sampling pulse one by one, as mentioned above, and this sampling pulse is supplied to sampling circuits SMP1-SMP40 (1st latch L1- 1- L1 -40). The video signal is inputted into sampling circuits SMP1-SMP40, and the video signal is held in each train to them according to the timing into which a sampling pulse is inputted. if maintenance of a video signal is completed to the last train in sampling circuits SMP1-SMP40 -- during a horizontal blanking interval -- the 2nd -- a latch pulse inputs into latch L2-1-L2-40 -- having -- the 1st -- the video signal currently held latch L1-1-L1-40 -- simultaneous -- the 2nd -- it is transmitted to latch L2-1-L2-40. that that is right, then the 2nd -- as for the video signal currently held latch L2-1-L2-40, one line is inputted into the data lines SA1-SA160 through sampling circuits SMP1-SMP40 at coincidence. and the 2nd -- while the video signal held latch L2-1-L2-40 is inputted into the data lines SA1-SA160, in shift registers SR1-SR40, a sampling pulse is outputted again. This actuation is repeated henceforth.
[0032]
The timing chart of said sampling circuits SMP1-SMP40 is shown in drawing 3 (C) here. As shown in drawing 3 (C), in two or more data lines arranged at each of SMP1-SMP40, a video signal is incorporated to coincidence.
[0033]
When the time-sharing drive of 15 subframes is displayed with the number SXGA of pixels and the clock frequency of a data driver is set to 5MHz like this operation gestalt, it can also become possible to carry out to more than 4microsec, and 1 horizontal-scanning period can fully be used.
[0034]
Subsequently, the example of a scanning-line driver is explained using drawing 3 (E). This scan driver has a shift register 310 and a buffer 311. If actuation is explained briefly, a shift register 310 will output a sampling pulse one by one, as mentioned above. The sampling pulse amplified with the buffer 311 after that is inputted into the scanning line, and it changes it into the selection condition one line at a time. And a video signal is written in the pixel controlled by the selected scanning line from the data line in order. In addition, you may make it the configuration which has arranged the level shifter between a shift register 310 and a buffer 311. By arranging a level shifter, the voltage swing of the logical-circuit section and the buffer section is changeable.
[0035]
This invention which has the above-mentioned configuration offers the display which canceled the lack of write-in time amount produced with enlargement and highly-minute-izing of a display, and its drive approach. Especially this invention offers the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the signal of a current value format by a digital time-sharing drive or analog drive.
[0036]
(Gestalt 2 of operation)
With the gestalt of this operation, about the pixel arranged at the i train of the j-th line of a picture element part E, some typical examples of a configuration are given and the configuration is explained using drawing 4 (A), (B), and drawing 10 (A) - (D). Drawing 10 (A) carries out the general expression

of a pixel circuit, and, as for the case of the video signal of an electrical-potential-difference format, in the case of the video signal of current formats, such as drawing 4 (A) and (B), drawing 10 (B) - (D) etc. is mentioned as an example.

[0037]

In drawing 4 (A) and (B), the gate electrode of the transistor 306 for a switch is connected to the scanning line Gj, the 1st source drain electrode is connected to a signal line Si, and the 2nd source drain electrode is connected to the gate electrode of the transistor 307 for a drive. The 1st source drain electrode of the transistor 307 for a drive is connected to the power-source line Vi, and the 2nd source drain electrode is connected to one electrode of a light emitting device 308. The electrode of another side of a light emitting device 308 is connected to the power-source line Cj.

[0038]

Moreover, in drawing 4 (B), it connects with a serial and the transistor 306 for a switch and the transistor 309 for elimination are arranged between the signal line Si and the power-source line Vi. The gate electrode of the transistor 309 for elimination is connected to the scanning line Rj. Here, the electrode of another side where one electrode of a light emitting device 308 connected to the 2nd source drain electrode of the transistor 307 for a drive was connected to the pixel electrode, the call, and the power-source line Cj is called a counterelectrode.

[0039]

In drawing 4 (A) and (B), the transistor 306 for a switch has the function which controls the input to the pixel of a video signal. Since the transistor 306 for a switch should just have the function as a switch, especially the conductivity type is not limited. Both an n channel mold and a p channel mold can be used.

[0040]

Moreover, in drawing 4 (A) and (B), the transistor 307 for a drive has the function which controls luminescence of a light emitting device 308. Although especially the conductivity type of the transistor 307 for a drive is not limited, when the transistor 307 for a drive is a p channel mold, it is desirable that a pixel electrode turns into an anode plate and a counterelectrode turns into cathode. Conversely, when the transistor 307 for a drive is an n channel mold, it is desirable that a pixel electrode turns into cathode and a counterelectrode turns into an anode plate.

[0041]

In drawing 4 (B), the transistor 309 for elimination has the function to make luminescence of a light emitting device 308 stop. Since the transistor 309 for elimination should just have the function as a switch, especially the conductivity type is not limited.

[0042]

In the pixel shown in above-mentioned drawing 4 (A) and (B), the signal of the format of an electrical potential difference is inputted into the gate electrode of the transistor 307 for a drive, and the drain current of the transistor 307 for a drive is supplied to a light emitting device 308.

[0043]

If it continues, as shown in drawing 10 (A), a current source 312 is arranged in a pixel and the pixel to which a predetermined current is supplied from this current source 312 at a light emitting device 308 is explained. A video signal is supplied from a signal line, a current is supplied from a power-source line, and, as for said current source 312, a control signal is supplied from the control line.

[0044]

In drawing 10 (B), transistors 313 and 314 have the function which controls the input of the signal to a pixel. Since the electrical potential difference between the gate sources of a transistor 315 is held by the capacitative element 317 at the predetermined electrical potential difference, a transistor 315 has the capacity to pass a predetermined drain current. The transistor 316 is controlling the flow with a light emitting device 308 and a transistor 315, and when a transistor 316 is ON, the drain current of a transistor 315 is supplied to a light emitting device 308. The circuit of drawing 10 (B) reproduces faithfully the signal current inputted into the pixel using a transistor 315, and has the advantage which can be supplied to a light emitting device 308. However, it is a difficulty that the current supplied to a

light emitting device and the signal current are not made to a different value.
[0045]
In drawing 10 (C), a transistor 318 has the function which controls the input of the signal to a pixel. Transistors 319 and 320 constitute current Miller circuit, and since the electrical potential difference between the gate sources of transistors 319 and 320 is held by the capacitative element 322 at the predetermined electrical potential difference, transistors 319 and 320 have the capacity to pass a predetermined drain current. A transistor 321 is arranged between the gate of a transistor 320, and the drain of a transistor 319. When the circuit of drawing 10 (C) changes a size ratio with transistors 319 and 320, it is an advantage that the ratio of the current and the signal current which are supplied to a light emitting device 308 can be set up freely. However, if the property of transistors 319 and 320 is not equal, the current supplied to a light emitting device 308 by the transistor 320 changes for every pixel, and there is a difficulty checked by looking as display nonuniformity.
[0046]
In drawing 10 (D), transistors 71-75 have the function which controls the input of the signal to a pixel. When writing a signal in a pixel, transistors 71-78 are turned ON and transistors 79 and 85 are turned OFF. Conversely, when supplying a current to a light emitting device 308, transistors 71-78 are turned OFF and transistors 79 and 85 are turned ON. The circuit of drawing 10 (D) has the advantage of the both sides of the circuit of drawing 10 (B) and (C).
[0047]
As for the transistor arranged at a pixel, two double-gate structures and a gate electrode may have [the gate electrode / not only one single gate structure but the gate electrode] multi-gate structures, such as three triple gate structures. Moreover, you may have which structure of the top gate structure where the gate electrode has been arranged in the upper part of a semi-conductor, and the bottom gate structure where the gate electrode has been arranged at the lower part of a semi-conductor. Moreover, although the pixel shown in drawing 4 (A) and (B) does not specify the capacitative element on the assumption that capacity coupling between the source gates of a transistor 307 is large, this invention may arrange the capacitative element which is not limited to this but holds the electrical potential difference between the gate sources of a transistor 307. Moreover, in a light emitting device 308, it has the structure where the luminous layer was inserted into an anode plate and cathode, and a list between said anode plates and said cathode. Said luminous layer is constituted by one or more ingredients chosen from an inorganic material, bulk materials, etc., such as an organic material and a carbon nano light.
[0048]
In addition, the power-source line Vi may be shared between the adjoining pixels. That is, it is not necessary to necessarily form a power-source line per 1 train, and the same power-source line can be shared between adjoining trains. In order that this invention may arrange two or more signal lines in one train, it is useful to improvement in a numerical aperture to share a power-source line between adjoining trains.
[0049]
However, in the display which performs color display, the brightness of the light emitted even if each pixel corresponding to each color of RGB arranged at 1 pixel impresses the same electrical potential difference by difference of the permeability of the current density of each ingredient of RGB, a color filter, etc. may differ. Therefore, the power-source line corresponding to each color is arranged in this case, and you may make it set up potential in each color. In addition, in this invention, 1 set of RGB is not called 1 pixel, but only by R, 1 pixel will be called only by 1 pixel and G, and 1 pixel will be called only by B.
[0050]
Subsequently, the actuation when applying a time-sharing drive to the display of this invention is explained using drawing 4 (C) - (E). Drawing 4 (C) In the timing chart shown in - (E), an axis of abscissa shows time amount, and an axis of ordinate shows the scanning line.
[0051]
In a time-sharing drive, an one-frame period is divided at two or more subframe periods SF. Each

subframe period SF has the elimination period Te in the write-in period Ta and the display period Ts or the write-in period Ta, and a display period Ts list.

[0052]

The elimination period Te is established at the subframe period SF which has the display period Ts shorter than the write-in period Ta. This is for making it the next write-in period Ta not begin immediately after termination of the display period Ts. It is because the two scanning lines will be chosen to the same timing and it becomes impossible to input a right signal into a pixel from a signal line after termination of the display period Ts temporarily, when the write-in period Ta is started immediately.

[0053]

In a time-sharing drive, the die length of the luminescence period in each subframe period SF shall be differed, and the combination of lighting of each subframe period SF or an astigmatism LGT expresses gradation. In the example shown in drawing 4 , the one-frame period is divided at five subframe periods SF1-SF5, using the number of gradation as 5 bits. And multi-tone is made to obtain the die length of the display periods Ts1-Ts5 which each subframe period has as a exponentiation of 2 like Ts1:Ts2:Ts3:Ts4:Ts 5= 16:8:4:2:1. That is, when expressing n bit gradation, the ratio of the die length of the display periods Ts1-Tsn is 2 (n-1):2 (n-2). : ... It is set to :21:20. And the write-in period Ta is a period which writes a digital video signal in each pixel, and is equal. [of the die length in each subframe period SF] The display period Ts is a period when a pixel performs lighting or an astigmatism LGT based on the video signal written in each pixel.

[0054]

Here, the pixel of drawing 4 (B) is mentioned as an example, and the actuation in each period of the elimination period Te is explained to the above-mentioned write-in period Ta and a display period Ts list.

[0055]

First, in the write-in period Ta, a pulse is inputted, and the scanning line Gj serves as H level, and turns on the transistor 306 for a switch. If it does so, the digital video signal outputted to the signal line Si will be inputted into the gate electrode of the transistor 307 for a drive.

Subsequently, in the display period Ts, when the transistor 307 for a drive turns on, a current flows and emits light to a light emitting device 308 according to the potential difference of the potential of the power-source line Vi, and the power-source line Cj. Moreover, when the transistor 307 for a drive is OFF, a current does not flow to a light emitting device 308, but serves as nonluminescent at it.

Then, in the elimination period Te, a pulse is inputted, the scanning line Rj serves as H level, and the transistor 309 for elimination turns it on. If the transistor 309 for elimination turns on, the electrical potential difference between the gate sources of the transistor 307 for a drive serves as zero, and the transistor 307 for a drive is turned off. If it does so, a current is no longer supplied to a light emitting device 308, and it will be in a nonluminescent condition. In addition, only the subframe period SF 5 is established at the elimination period Te. In the subframe period SF 5, since this has the display period Ts5 shorter than the write-in period Ta 5, it is for making it the next write-in period not begin immediately after termination of this display period Ts5.

[0056]

In the timing chart of drawing 4 , although the subframe periods SF1-SF5 had appeared in order, this invention is not limited to this. A subframe period may appear at random. Moreover, in order to control display active jamming of a false profile etc., the subframe period of arbitration may be divided and may be made to appear.

[0057]

This invention which has the above-mentioned configuration offers the display which canceled the lack of write-in time amount produced with enlargement and highly-minute-izing of a display, and its drive approach. Especially this invention offers the display which canceled the remarkable lack of write-in time amount, and its drive approach, when using the signal of a current value format by a digital time-sharing drive or analog drive.

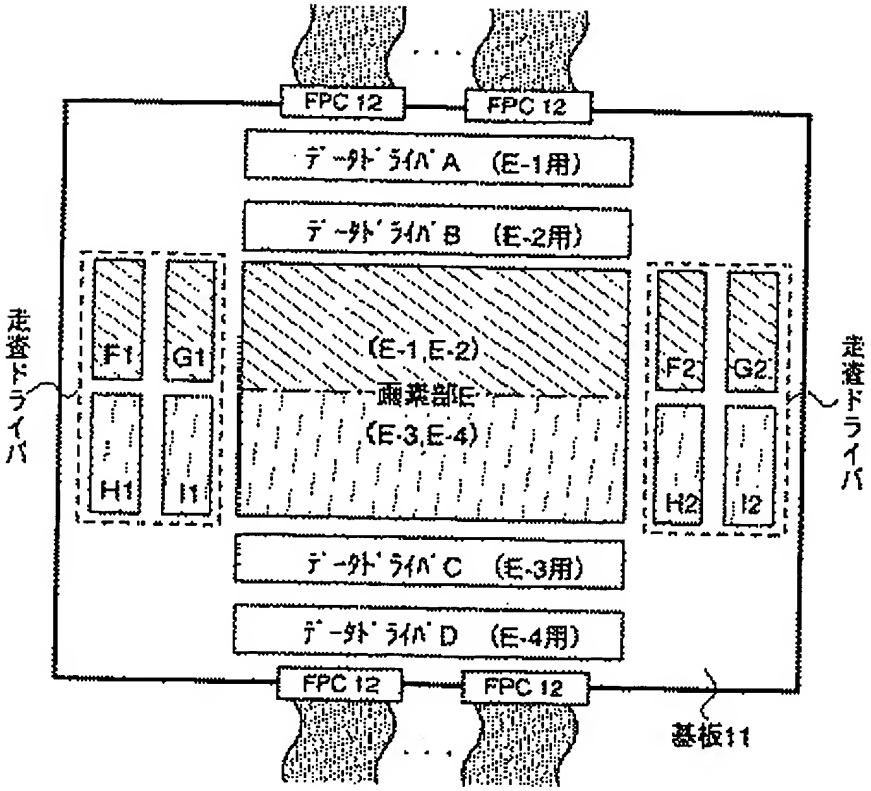
[0058]
The gestalt of this operation can be combined with the gestalt 1 and arbitration of operation.
[0059]
(Gestalt 3 of operation)
The gestalt of this operation explains the layout plan of the pixel at the time of applying the circuit shown in drawing 4 (A) to the gestalt shown in drawing 2 using drawing 5 .
[0060]
To drawing 5 , four pixels of a pixel E-1 to E-4 are illustrated, data-line SAi-SDi is arranged in the direction of a train, and scanning-line Gj-G (j+3) is arranged at the line writing direction. Each pixel has TFT for a switch, TFT for a drive, and a capacity object. Although the light emitting device connected to TFT for a drive is equivalent to a pixel electrode and a luminous layer list at the layered product of a counterelectrode, it is illustrating only the pixel electrode in drawing 5 .
[0061]
Although TFT for a switch is considering as the double-gate mold transistor, this invention may not be limited to this, may be a single gate mold, or may be the multi-gate mold of the number of arbitration. Moreover, the capacity object is formed among drawing with the insulator arranged in the meantime at the metal body list formed in the same layer as a power-source line and a gate electrode as a means for holding the electrical potential difference between the gate sources of TFT for a drive. However, with the parasitic capacitance of gate capacitance of TFT own [for a drive] and channel capacity, wiring, etc., when it is possible to hold the electrical potential difference between the gate sources of TFT for a drive, it is not necessary to newly arrange a capacity object.
[0062]
The gestalt of this operation can be combined with the gestalten 1 and 2 and arbitration of operation.
[0063]
(Gestalt 4 of operation)
As electronic equipment by which this invention is applied, a video camera, a digital camera, A goggles mold display (head mount display), a navigation system, Sound systems (a car audio, audio component stereo, etc.), a note type personal computer, A game device, a Personal Digital Assistant (a mobile computer, a cellular phone, a handheld game machine, or digital book), The picture reproducer (equipment equipped with the display which specifically reproduces record media, such as Digital Versatile Disc (DVD), and can display the image) equipped with the record medium etc. is mentioned. The example of those electronic equipment is shown in drawing 6 .
[0064]
Drawing 6 (A) is luminescence equipment and contains a case 2001, susceptor 2002, a display 2003, the loudspeaker section 2004, and video input terminal 2005 grade. This invention is applicable to a display 2003. Moreover, the luminescence equipment shown in drawing 6 (A) is completed by this invention. Since it is a spontaneous light type, luminescence equipment has an unnecessary back light, and it can be made into a display thinner than a liquid crystal display. In addition, as for luminescence equipment, all the displays for information displays the object for personal computers, the object for TV broadcast reception, for an advertising display, etc. are contained.
[0065]
Drawing 6 (B) is a digital still camera, and contains a body 2101, a display 2102, the television section 2103, the actuation key 2104, the external connection port 2105, and shutter 2106 grade. This invention is applicable to a display 2102. Moreover, the digital still camera shown in drawing 6 (B) is completed by this invention.
[0066]
Drawing 6 (C) is a note type personal computer, and contains a body 2201, a case 2202, a display 2203, a keyboard 2204, the external connection port 2205, and pointing mouse 2206 grade. This invention is applicable to a display 2203. Moreover, the luminescence equipment shown in drawing 6 (C) is completed by this invention.
[0067]

Drawing 6 (D) is a mobile computer and contains a body 2301, a display 2302, a switch 2303, the actuation key 2304, and infrared port 2305 grade. This invention is applicable to a display 2302. Moreover, the mobile computer shown in drawing 6 (D) is completed by this invention.
[0068]
Drawing 6 (E) is the picture reproducer (specifically DVD regenerative apparatus) of the pocket mold equipped with the record medium, and contains a body 2401, a case 2402, a display A2403, a display B2404, the record-media (DVD etc.) reading section 2405, the actuation key 2406, and loudspeaker section 2407 grade. although a display A2403 mainly displays image information and a display B2404 mainly displays text -- this invention -- Displays A and B -- it is applicable to 2403 and 2404. In addition, a home video game machine machine etc. is contained in the picture reproducer equipped with the record medium. Moreover, the image display device shown in drawing 6 (E) by this invention is completed.
[0069]
Drawing 6 (F) is a goggles mold display (head mount display), and contains a body 2501, a display 2502, and the arm section 2503. This invention is applicable to a display 2502. Moreover, the goggles mold display shown in drawing 6 (F) is completed by this invention.
[0070]
Drawing 6 (G) is a video camera and contains a body 2601, a display 2602, a case 2603, the external connection port 2604, the remote control receive section 2605, the television section 2606, a dc-battery 2607, the voice input section 2608, and actuation key 2609 grade. This invention is applicable to a display 2602. Moreover, the video camera shown in drawing 6 (G) is completed by this invention.
[0071]
Drawing 6 (H) is a cellular phone and contains a body 2701, a case 2702, a display 2703, the voice input section 2704, the voice output section 2705, the actuation key 2706, the external connection port 2707, and antenna 2708 grade. This invention is applicable to a display 2703. In addition, a display 2703 can stop the consumed electric current of a cellular phone by displaying a white alphabetic character on a black background. Moreover, the cellular phone shown in drawing 6 (H) is completed by this invention.
[0072]
In addition, if high brightness luminescence use will be attained by the advance of luminescent material in the future, it will also become possible to carry out expansion projection of the light containing the outputted image information with a lens etc., and to use for the projector of a front mold or a rear mold.
[0073]
Moreover, the above-mentioned electronic equipment displays more often the information distributed through electronic communication lines, such as the Internet and CATV (cable television), and its opportunity to display especially animation information has been increasing. Since the speed of response of luminescent material is very high, luminescence equipment is desirable to a movie display.
[0074]
Moreover, in order that the part which is emitting light may consume power, as for luminescence equipment, it is desirable to display information that the amount of light-emitting part decreases as much as possible. Therefore, when using luminescence equipment for the display which is mainly concerned with text like a Personal Digital Assistant especially a cellular phone, or a sound system, it is desirable to drive so that text may be formed by part for a light-emitting part by making a nonluminescent part into a background.
[0075]
As mentioned above, the applicability of this invention is very wide, and using for the electronic equipment of all fields is possible. Moreover, the display of which configuration shown in the gestalten 1-3 of operation may be used for the electronic equipment of the gestalt of this operation.
[0076]
(Gestalt 5 of operation)
The module in the condition that IC which includes a controller, a power circuit, etc. in the panel in the condition that the closure of the light emitting device was carried out was mounted in the electronic

equipment shown in the gestalt 4 is carried. Both a module and a panel are equivalent to one gestalt of a display. Here, the modular concrete example of a configuration is explained.
[0077]
The external view of the module with which the controller 801 and the power circuit 802 were mounted in the panel 800 by drawing 11 (A) is shown. The scanning-line drive circuit 804 which chooses as a panel 800 the pixel which the picture element part 803 by which the light emitting device was prepared in each pixel, and said picture element part 803 have, and the signal-line drive circuit 805 which supplies a video signal to the selected pixel are formed.
[0078]
Moreover, the controller 801 and the power circuit 802 are established in the printed circuit board 806, and the various signals and supply voltage which were outputted from the controller 801 or the power circuit 802 are supplied to the picture element part 803 of a panel 800, the scanning-line drive circuit 804, and the signal-line drive circuit 805 through FPC807.
[0079]
The supply voltage and the various signals to a printed circuit board 806 are supplied through the interface (I/F) section 808 by which two or more input terminals have been arranged.
[0080]
In addition, although a printed circuit board 806 uses FPC for a panel 800 and is mounted in it in this example, it is not necessarily limited to this configuration. You may make it make a controller 801 and a power circuit 802 mount in a panel 800 directly using a COG (Chip on Glass) method.
[0081]
Moreover, in a printed circuit board 806, by resistance which the capacity formed between wiring of leading about and the wiring itself have, a noise may take supply voltage and a signal or the standup of a signal may become blunt. Then, you may make it prevent preparing various components, such as a capacitor and a buffer, in a printed circuit board 806, and a noise's taking supply voltage and a signal or the standup of a signal becoming blunt.
[0082]
A block diagram shows the configuration of a printed circuit board 806 to drawing 11 (B). The various signals and supply voltage which were supplied to the interface 808 are supplied to a controller 801 and supply voltage 802.
[0083]
The controller 801 has the analog interface circuitry 809, phase lock DORUPU (PLL:Phase Locked Loop) 810, the control signal generation section 811, and SRAM (Static Random Access Memory) 812 and 813. In addition, it is DRAM (Dynamic Random) if writing and read-out of data are possible at SDRAM and a high speed instead of SRAM, although SRAM is used in this example.
Access It is possible to also use Memory.
[0084]
The analog video signal supplied through the interface 808 is inputted into the control signal generation section 811 in the analog interface circuitry 809 as an AD translation and digital video signal corresponding to [parallel serial conversion is carried out and] each color of R, G, and B. Moreover, based on the various signals supplied through the interface 808, in the analog interface circuitry 809, a Hsync signal, a Vsync signal, a clock signal CLK, etc. are generated, and it is inputted into the control signal generation circuit 811. However, when a direct digital video signal is inputted into an interface 808, the analog interface circuitry 809 does not need to arrange.
[0085]
In phase lock DORUPU 810, it has the function to double the phase of the frequency of the various signals supplied through an interface 808, and the clock frequency of the control signal generation circuit 811. Although the clock frequency of the control signal generation circuit 811 is not necessarily the same as the frequency of the various signals supplied through the interface 808, it adjusts the clock frequency of the control signal generation circuit 811 in phase lock DORUPU 810 so that it may synchronize mutually.

[0086]
The video signal inputted into the control signal generation circuit 811 is once written in SRAM 812 and 813, and is held. In the control signal generation circuit 811, every 1 bit of video signals corresponding to all pixels is read among the video signals of all the bits currently held at SRAM812, and the signal-line drive circuit 805 of a panel 800 is supplied.
[0087]
Moreover, in the control signal generation circuit 811, the information about the period when the light emitting device of each bit emits light is supplied to the scanning-line drive circuit 804 of a panel 800.
[0088]
Moreover, a power circuit 802 supplies predetermined supply voltage to the signal-line drive circuit 805, the scanning-line drive circuit 804, and picture element part 803 of a panel 800.
[0089]
Next, the detailed configuration of a power circuit 802 is explained using drawing 12 . A power circuit 802 consists of a switching regulator 854 which used four switching regulator control 860, and a series regulator 855.
[0090]
Generally, the switching regulator is small and lightweight compared with a series regulator, and not only pressure lowering but can also carry out [a pressure up or] positive/negative reversal. On the other hand, although a series regulator is used only for pressure lowering, compared with a switching regulator, the precision of output voltage is good, and a ripple and a noise are hardly generated. In the power circuit 802 of this example, it uses combining both.
[0091]
drawing 12 -- being shown -- a switching regulator -- 854 -- a switching regulator -- control (SWR) -- 860 -- attenuator (attenuator: ATT) -- 861 -- a transformer -- (-- T --) -- 862 -- an inductor -- (-- L --) -- 863 -- a reference supply (Vref) -- 864 -- an oscillator circuit (OSC) -- 865 -- diode -- 866 -- a bipolar transistor -- 867 -- variable resistance -- 868 -- capacity -- 869 -- having -- **** .
[0092]
By the electrical potential difference of external Li ion cell (3.6V) etc. being changed in a switching regulator 854, the supply voltage given to cathode and the supply voltage supplied to a switching regulator 854 are generated.
[0093]
Moreover, a series regulator 855 has the band gap circuit (BG) 870, amplifier 871, an operational amplifier 872, a current source 873, variable resistance 874, and a bipolar transistor 875, and the supply voltage generated in the switching regulator 854 is supplied.
[0094]
In a series regulator 855, the supply voltage of the direct current given to wiring (current supply source line) for supplying a current to the anode plate of the light emitting device of each color based on the fixed electrical potential difference generated in the band gap circuit 870 using the supply voltage generated in the switching regulator 854 is generated.
[0095]
In addition, in the case of the drive method with which the current of a video signal is written in a pixel, a current source 873 is used. In this case, the current generated in the current source 873 is supplied to the signal-line drive circuit 805 of a panel 800. In addition, in the case of the drive method with which the electrical potential difference of a video signal is written in a pixel, it is not necessary to necessarily establish a current source 873.
[0096]

[Translation done.]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H1
I1
(E-1,E-2)
画素部E
(E-3,E-4)
F2
G2
H2
I2
走査ドライバ
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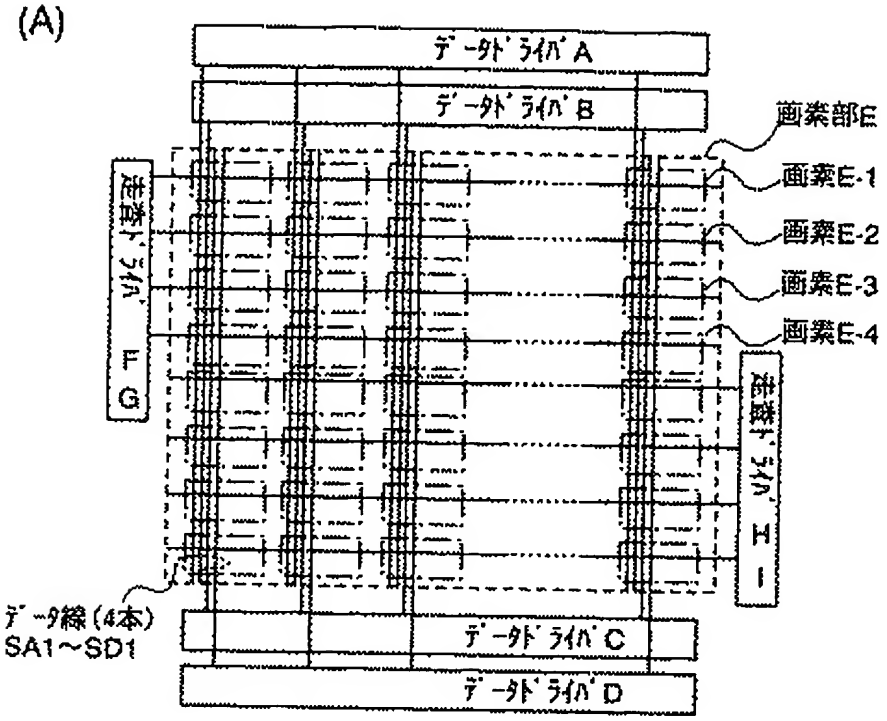
FPC 12
基板11

(A)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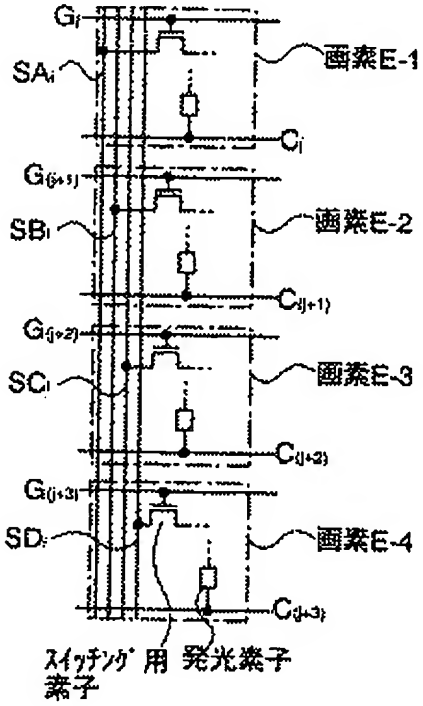
データドライバ C
データドライバ D

(B)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SDi
画素E-4
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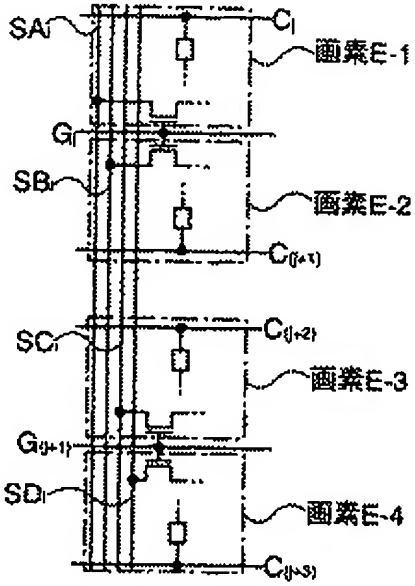
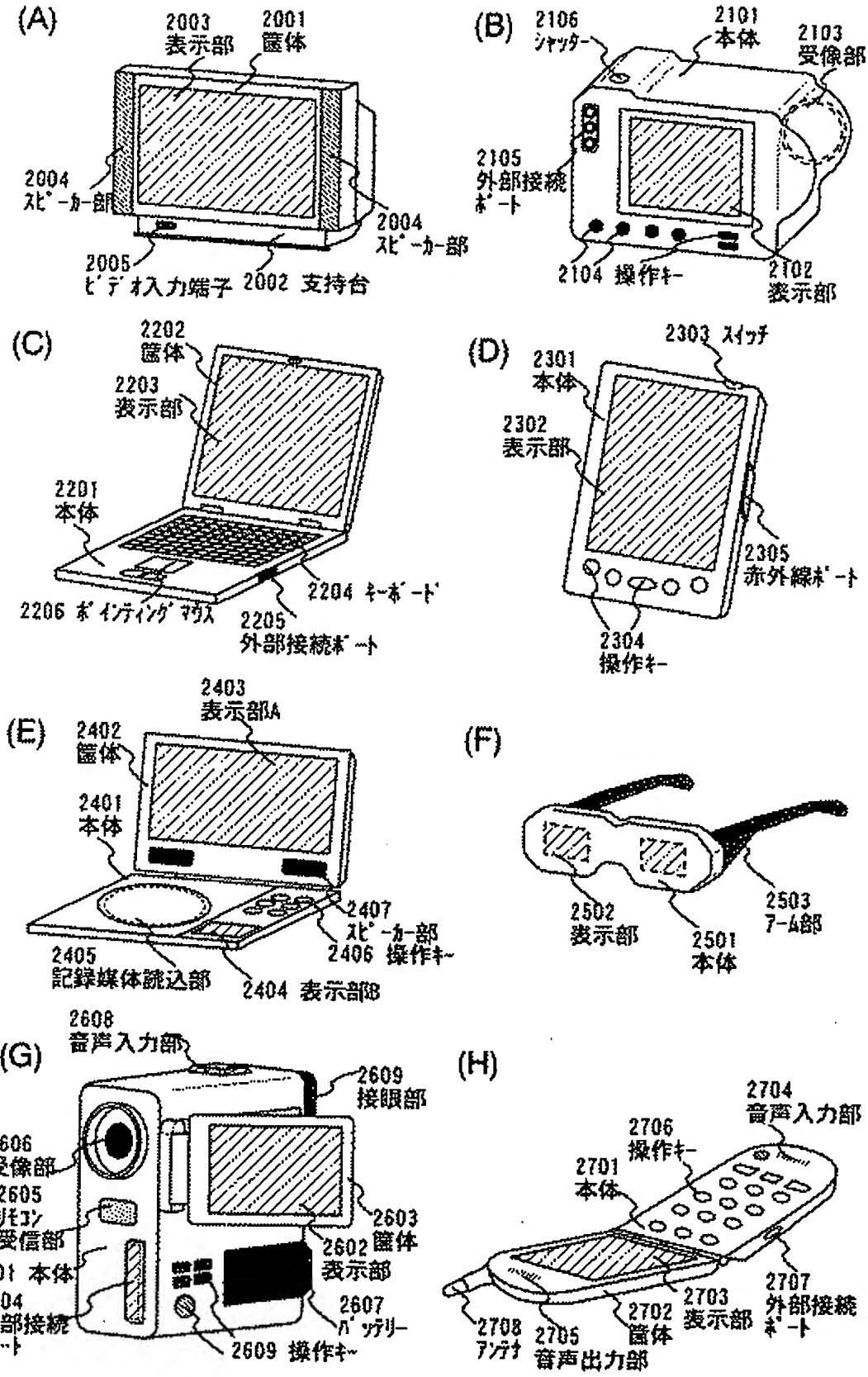
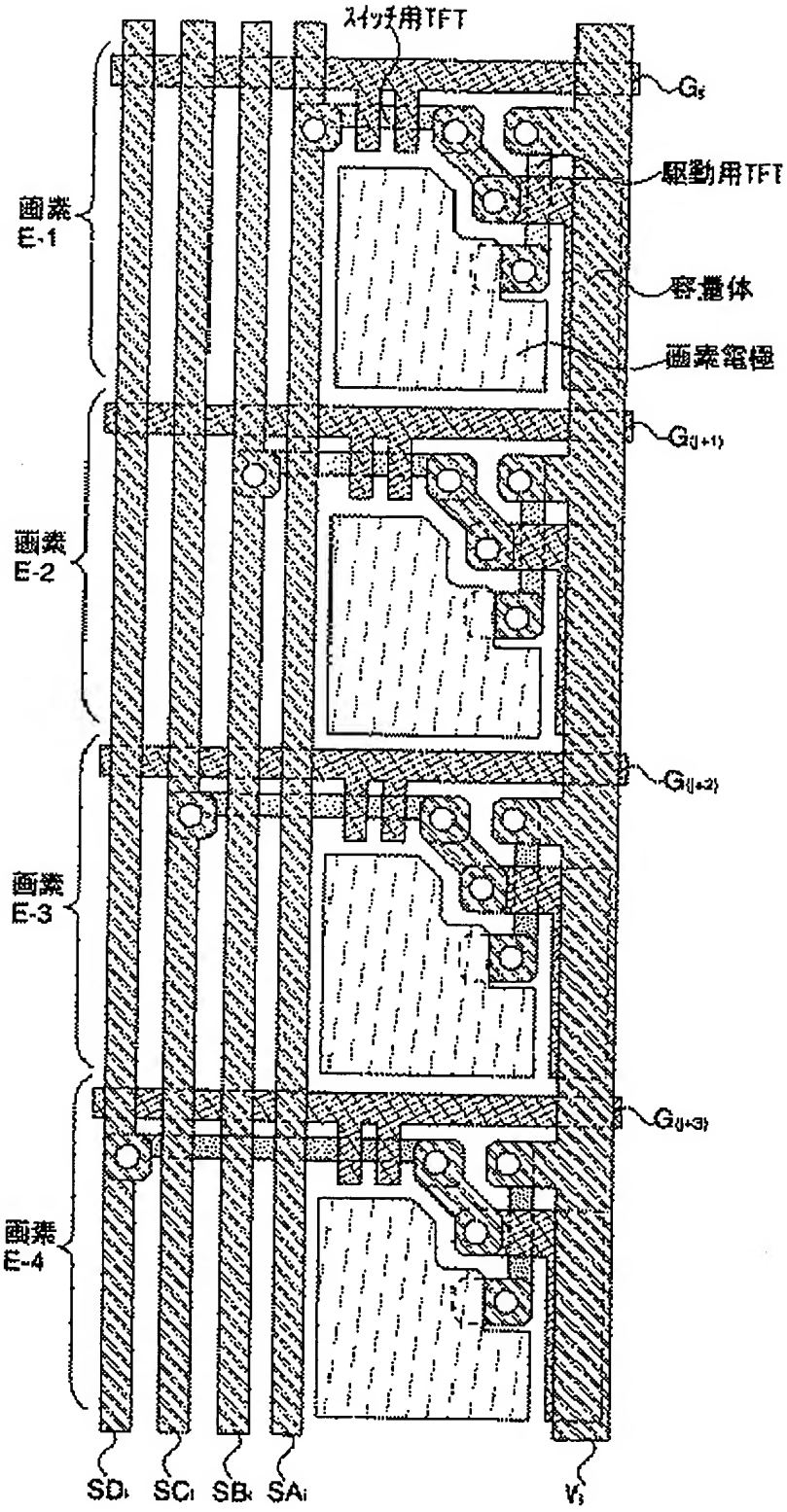
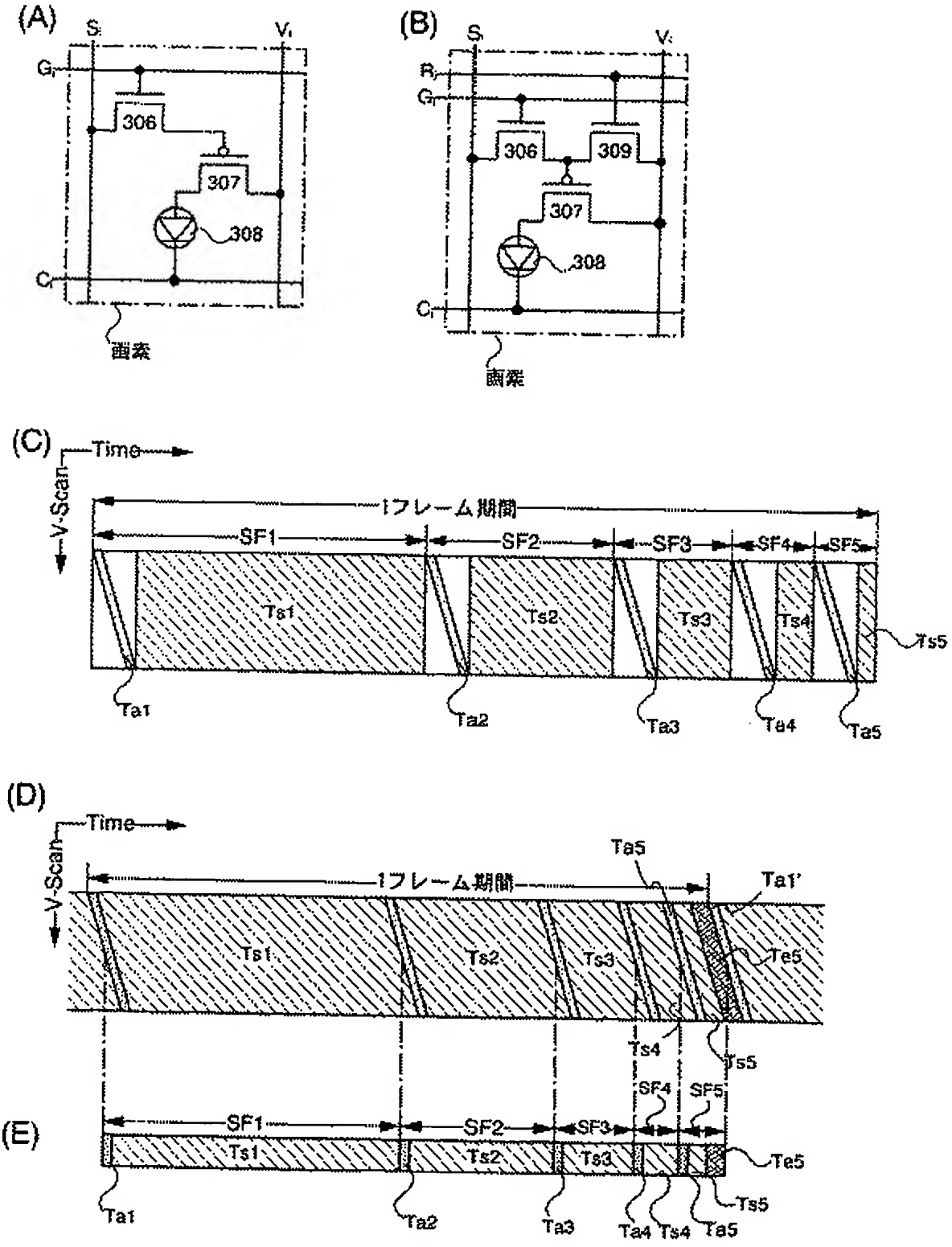
スイッチング用素子
発光素子

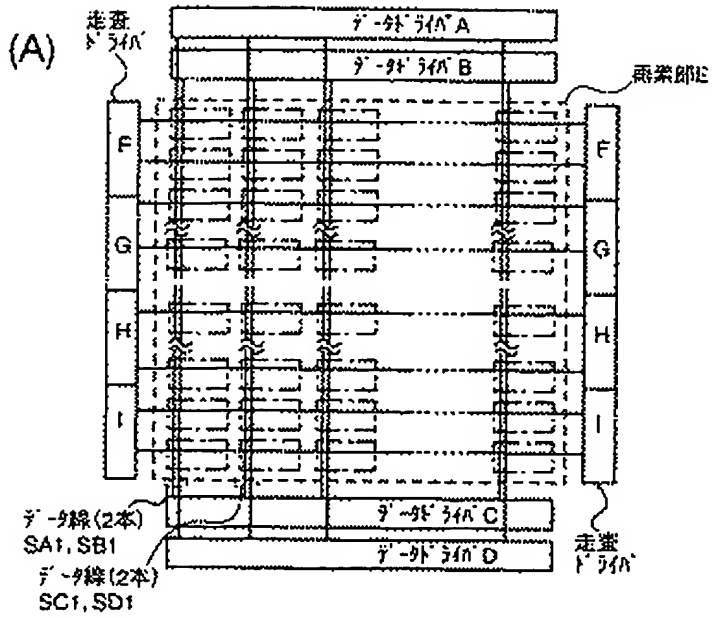
(C)

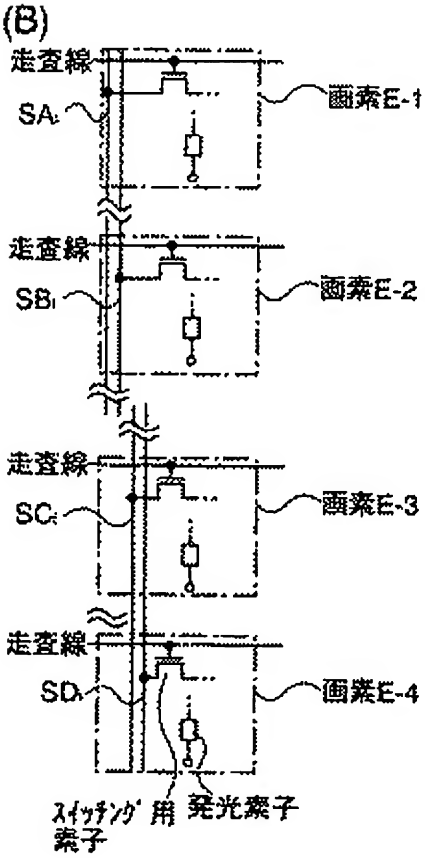

SAi
Ci
画素E-1
Gi
SBi
画素E-2
C(j+1)
SCi
C(j+2)
画素E-3
G(j+1)
SDi
画素E-4
C(j+3)

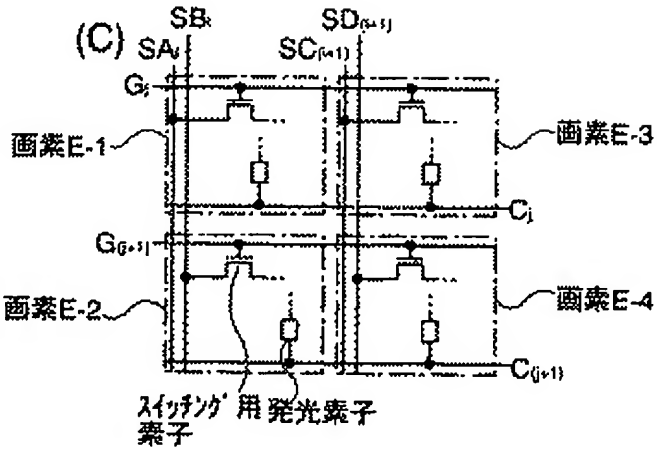

(A)
2003 表示部
2001 筐体
2004 スピーカー部
2004 スピーカー部
2005 ビデオ入力端子
2002 支持台
(B)
2106 シャッター
2101 本体
2103 受像部
2105 外部接続ポート
2104 操作キー
2102 表示部
(C)
2202 筐体
2203 表示部
2201 本体
2204 キーボード
2206 ポインティングマウス
2205 外部接続ポート
(D)
2303 スイッチ
2301 本体
2302 表示部
2305 赤外線ポート
2304 操作キー
(E)
2403 表示部A
2402 筐体
2401 本体
2407 スピーカー部
2406 操作キー
2405 記録媒体読込部
2404 表示部B
(F)
2503 アーム部
2502 表示部
2501 本体
(G)
2608 音声入力部
2609 接眼部
2606 受像部
2605 リモコン受信部
2603 筐体
2602 表示部
2601 本体
2607 バッテリー
2604 外部接続ポート
2609 操作キー
(H)
2704 音声入力部
2706 操作キー
2701 本体
2707 外部接続ポート
2703 表示部
2702 筐体
2708 アンテナ
2705 音声出力部


スイッチ用TFT
G_i
駆動用TFT
画素
E-1
容量体
画素電極
$G_{(i+1)}$
画素
E-2
$G_{(i+2)}$
画素
E-3
$G_{(i+3)}$
画素
E-4
SD_i
SC_i
SB_i
SA_i
V_i


(A)
(B)
306
307
308
309
画素
(C)
Time
V-Scan
1フレーム期間
SF1
SF2
SF3
SF4
SF5
Ts1
Ts2
Ts3
Ts4
Ts5
Ta1
Ta2
Ta3
Ta4
Ta5
(D)
Ta1'
Te5
(E)


(A)
走査ドライバ
データドライバ A
データドライバ B
画素部
F
G
H
I
データ線(2本)
SA1, SB1
データ線(2本)
SC1, SD1
データドライバ C
データドライバ D
走査ドライバ


(B)
走査線
SAi
画素E-1
走査線
SBi
画素E-2
走査線
SCi
画素E-3
走査線
SDi
画素E-4
スイッチング用素子
発光素子


(C)
SBi
SD(j+1)
SAi
SC(j+1)
Gi
画素E-1
画素E-3
Cj
G(i+1)
画素E-2
画素E-4
C(j+1)
スイッチング用素子
発光素子